



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,442	12/04/2001	Chun-Liang Lee	3313-0431P-SP	9178
2292	7590	02/09/2005	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			LIN, KELVIN Y	
			ART UNIT	PAPER NUMBER

2142

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/000,442	Applicant(s) LEE, CHUN-LIANG	
	Examiner Kelvin Lin	Art Unit 2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

Detailed Action

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. In Claim 13, the phrase "ROM unit is a ROM" is ambiguous.
2. The above noted problems are not necessarily an exhaustive listing, but are meant to be exemplary of the types of errors present. It is incumbent upon an applicant to ensure that any amendment filed resolves all deficiencies and places the claims in compliance with 35 USC 112.
3. Appropriate correction is required

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5-11, 13-15, and 18 are rejected under 35 USC 102(b) as being anticipated by Kumar et al., (U.S. Patent 5970069).

3. Regarding claim 1, Kumar teaches a transmission management device of a server implemented with a serial port RS232 and a bus, the transmission management device comprising:

- a transmission system connected with an independent sub-system of the server for receiving and storing data and commands of the server and for transmitting the data and the commands of the server to the independent sub-system (Kumar, Fig.2a, col.4, l.58-67,col. 1-6, col.8, l.17-39);
- a control system connected with the transmission system for receiving data and commands from an external system and interrupt signals of the server and for transmitting the information, commands and interrupt signals to the independent sub-system through the bus (Kumar, Fig.2a, col.4, l.32-43); and

- an I/O system connected with the external system for transmitting the data and the commands of the external system to the transmission system and the control system, and for transmitting the data and the commands of the server to the external system (Kumar, col.5, l.19-36).

4. Regarding claim 2, Kumar further discloses the transmission management device of claim 1, wherein the transmission system comprises:

- a connecting unit connected with the independent sub-system for connections with the independent sub-system and for transmitting the data and the commands of the server (Kumar, Fig.2a, col.4, l.53-57);
- a control unit connected with the connecting unit for temporarily storing and converting the data and the commands to asynchronous signals, for transmitting the asynchronous signals to the connecting unit, and for transmitting the interrupt signal to a CPU (Kumar, col.6, l.48-55, col.8, l.3-5, col.27, l.24); and
- a decoding unit connected with the control system for receiving the data transmitted from the control system and for transmitting the information to the control unit after decoding (Kumar, col.8, l.45-57)

5. Regarding claim 3, Kumar further discloses the transmission management device of claim 2, wherein the connecting unit is a serial port RS232 connecting device

(Kumar, col.1, l.20, col.4, l.44).

6. Regarding claim 5, Kumar further discloses the transmission management device of claim 1, wherein the control system comprises:

- a network connector for connecting with the external system (Kumar, col.4, l. 53-57);
- a system control unit connected with the network connector for transmitting the data and the commands of the external system and the interrupt signals to the transmission system and to the independent sub-system through the bus (Kumar, Fig.15, col.6, l.56-67) ; and
- a memory unit connected with the system control unit for storing the data and the commands of the external system (Kumar, col.7, l. 25-40).

7. Regarding claim 6, Kumar further discloses the transmission management device of claim 5, wherein the system control unit is a SOC (System On Chip) (Kumar, col.5, l.17-20).

8. Regarding claim 7, Kumar further discloses the transmission management device of claim 5, wherein the memory unit is a SDRAM (Synchronous Dynamic Random Access Memory) (Kumar, col.6, l.61).

9. Regarding claim 8, Kumar further discloses the transmission management device of claim 5, wherein a PCI Bus is installed between the network connector and the system control unit (Kumar, col.7, l.1-6).

10. Regarding claim 9, Kumar further discloses the transmission management device of claim 5, wherein a memory bus is installed between the control unit and the memory unit (Kumar, col.7, l.6-10).
11. Regarding claim 10, Kumar further discloses the transmission management device of claim 5, wherein a data bus is installed between the transmission system and the control system (Kumar, col.6, l.2-9).
12. Regarding claim 11, Kumar further discloses the transmission management device of claim 1, wherein the I/O system contains:
 - a receiving unit connected with the external system (Kumar, Fig.5, col.9, l.9-24))
 - an I/O unit connected with the receiving unit for receiving the data and the commands of the external system and transmitting the data and the commands to the transmission system and the control system (Kumar, col.8, l.1-39); and
 - a ROM unit connected with the bus for storing the data and the commands of the server (Kumar, Fig.5, component 164).
13. Regarding claim 13, Kumar further discloses the transmission management device of claim 11, wherein the ROM unit is a ROM (Kumar, col.9, l.28-31).
14. Regarding claim 14, Kumar further discloses the transmission management device of claim 1, wherein the interrupt signals are transmitted to the CPU by parallel connections (Kumar, col.7, l.8-10).

15. Regarding claim 15, Kumar further discloses the transmission management device of claim 1, wherein the interrupt signals are transmitted to the CPU by serial connections (Kumar, Fig.3, component 70, col.7, l.6-7).
16. Regarding claim 18, Kumar further discloses the transmission management device of claim 5, wherein the system control unit transmits the data and the commands of the external system to the transmission system through the decoding unit (Kumar, col. 5, l.38-41).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. Claims 4, and 12 are rejected under 35 U.S.C 103(a) as being unpatentable over Kumar in view of Mergard et al., (US Patent 6401156).
18. Regarding claims 4, and 12, Kumar differs from the claimed invention in that it does not explicitly indicate the transmission management device of claim 2, wherein the control unit is an UART (Universal Asynchronous Receiver/Transmitter) with a FIFO (First-In-First-Out) function; Similarly, Kumar does not explicitly indicate transmission management device of claim 12, wherein the I/O unit is a super I/O. However, Mergard clearly teaches that a UART block includes two PC16550-compatible UARTs, both capable of running 16450 and 16550 software. The UART block supports DMA operation, a FIFO mode, an internal baud rate clock to handle baud rates up to 1.5 M bits/s, false start bit detection, break detection, full-duplex operation, and other features (Mergard, col.7, l.32-37). In addition, the external sources include devices connected to the PCI bus or the general purpose bus. The interrupt router and the interrupt router may receive interrupts from internal sources including the AMDeug, the address decode unit, the programmable interval timers,

the UARTs for the control unit. (Mergard, col.10, l.26-36). Furthermore, Mergard clearly teaches that a the super I/O chip implements two UARTs programmed at the same address as the integrated UARTs of the microcontroller, the internal UARTs maybe disabled to support the UARTs in the super I/O chip if desired. In this case, when the processor performs I/O access to the UART address regions, the cycles are forwarded to the external general purpose bus for the I/O controller. Therefore, under PCI architecture, combine with Kumar's I/O control unit with Mergard's UART with FIFO, and super I/O interface would have been obvious to one of ordinary skill in the art at the time the invention was made.

19. Claims 16, and 17 are rejected under 35 U.S.C 103(a) as being unpatentable over Kumar in view of Mergard as applied to claim 4, and 12. and further in view of Brown et al., (US Patent 6845410).
20. Regarding claims 16, and 17, Kumar as modified by Mergard lacks combination with transmission management device that the bus contains an I2C bus switching device for switching the bus signals, thereby transmitting the signals to the different independent sub-systems.
21. However, Brown teaches that controller 20 includes a CPU 21, for example a Motorola ColdFire brand 32-bit MCU, connected to an I2C bus Controller includes a plurality of ports, including a RS-232 port for connection to a console display for displaying diagnostic and other

information the system management port I2C task manages communication between a I2C device and the controller.

The I2C task will receive request, response and event packets from packet router. In one embodiment, the packets are temporarily buffered in queues 1161 and 1163 between the router and the I2C task. The I2C task unencapsulates the I2C data from the packet and transmits the I2C data to the I2C device. The I2C task also receives transmissions from the I2C device, encapsulates the data in a packet, and transmits the packet to the router (Brown, col.5, l. 41-56). That means modify the Kumar's RS-232 interface will transmit the signals to the different independent sub-system via RS-232

22. Therefore, based on RS-232 interface and combine with Kumar's RS232, PCI, unit with Brown's I2C bus device, and would have been obvious to one of ordinary skill in the art at the time the invention was made:

Conclusion

The prior art made of record and not relied upon is considered pertinent to application's disclosure.

- Chaiken G., (Patent No. 6128732) Implementing Universal Serial Bus Support With a Minimum of System RAM.
- Berglund et al., (Patent No. 6351819) Heterogeneous System Enclosure Service Connection.
- Ha et al., (Patent No. 6490638) General Purpose Bus with Programmable Timing.
- IEEE – Freear S. An Intravascular Ultrasound Imaging System, IEEE Multiprocessor DSP – Application, Algorithm and Architecture, IEE Colloquium on 31 May 1995, pp. 1-5.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelvin Lin whose telephone number is 571-272-3898. The examiner can normally be reached on Flexible 4/9/5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Harvey can be reached on 571-272-3896. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2142

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/26/05
KYL

Jack Hunsy
SUPERVISOR OF FIELD EXAMINERS